RECENT RESULTS USING MET-VIA TSV INTERPOSER TECHNOLOGY AS TMV ELEMENT IN WAFER LEVEL THROUGH MOLD VIA PACKAGING OF CMOS BIOSENSORS

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ABSTRACT

This paper reports on the successful manufacture of metalized TSV interposer technology as a through molded via element in wafer level packaging of CMOS biosensors. The work has been executed by Silex Microsystems and Fraunhofer IZM, within the EU-consortium CAJAL4EU, where originally 29 partners were developing nanoelectronics-based biosensor technology platforms [1]. The finished metalized TSV interposers fabricated by Silex's 8" line were electrically characterized before molding and showed low resistance (mean resistance 10.3mΩ/Via, with σ of 2.4) and a high yield of 99.6 %.The Chip in Polymer (CiP) Reconfigured wafers was fabricated by IZM. The TSV interposers and CMOS biosensor chips die were interconnected using a PCB based redistribution allowing low-cost heterogeneous integrated packaging and separation between the active biosensor with wet I/Os and the dry electrical connections.

The finished assembled package with the bio-sensor were optically inspected by X-ray CT, X-ray, cross sectioning and SEM. Preliminary results indicates that the complete molded module has an electrical contact, from top-bottom-top, with a resistance of 1-3Ω.

Key words: MEMS Manufacturing, Interposer, TSV, TMV, Wafer Level Packaging, Vacuum Molding, Polymer package, Reconfigured wafers, Heterogeneous Integration, biosensors, CMOS biosensor.

INTRODUCTION

Due to the aging society and the raising of health standards in the more developed countries, the healthcare costs per capita increase much more rapidly than the Gross Domestic Product (GDP) per capita. Presently, there is a clear driver towards prevention to reduce healthcare costs and to increase the quality of life, which demands technologies with functionalities beyond traditional diagnostic methodologies, namely on-the-spot or point-of-care (PoC) diagnostics instead of analysis in a centralized lab. In the CAJAL4EU consortium under the European ENIAC Joint undertaking initiative the objective was to bridge this gap by novel and advanced technologies. The project coordinated by NXP, Belgium aimed at developing microelectronic-based diagnostic biosensor platforms, enabling in-vitro diagnostics for a variety of new multi-parameter test applications in a robust, user-friendly and cost-effective way. The technology is based on nano-electronic modules, where micro-electronic based diagnostic detection platforms increase sensitivity, specificity and multiplex capability in human body fluid diagnostics, allowing prototype experiments, which could be performed at the bedside, in the clinic, in an ambulance, at emergency rooms or at home depending on the particular needed diagnostic question [1].

The biosensors consist of a nanoelectronic-based CMOS transducer with an interface chemistry which makes the connection to the clinical sample to be analyzed. Subsequently, capturing of bio-targets can be detected by measuring capacitive/impedance changes in the electrical signal. With on-chip detection electronics, small electrical changes can be detected within milliseconds, enabling massively parallel real-time monitoring of bio-molecule binding events, illustrated in Figure 1. Besides the transducers, interface chemistry and spotting technologies, microfluidics, software and hardware developments (and their integration) have been developed by other CAJAL4EU partners to realize fully integrated biosensor systems and lab-on-chip devices. The detection principle for the biosensors is electrical-detection (CMOS-based) by use of capacitive/impedance or electrochemical sensing strategies. These method exhibit a high potential towards rapid, highly sensitive multiplexed detection of biomolecules, preferably label-free [1].

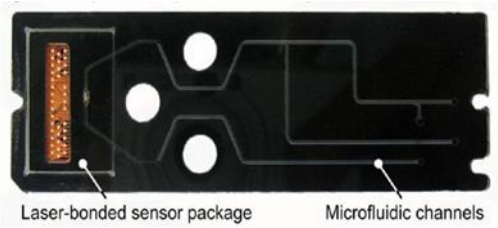

Figure 1 *Microfluidic flow cell, with laser-bonded polymeric multi-layer stack illustrating one of the approaches in CAJAL4EU, for the integration of CMOS biosensor into a polymeric lab-on-a-chip system [2].*

The focus for Silex Microsystems and Fraunhofer IZM within this CAJAL4EU project has been to develop a novel heterogeneous integration packaging techniques between the active biosensor and the electrical connections. The metalized Through-Silicon-Vias (TSV) interposer will establish the electrical connection between

the microfluidics and the control unit and due to the hermetic seal of the vias a *well-defined separation* of the microfludic from the electrical connection is realized. For this approach, dies with TSV manufactured by Silex [3] were assembled at Fraunhofer IZM, together with the active biosensor. After compression molding only the active biosensor and one side of TSV dies are accessible for thin film interconnection. Therefore, the redistribution of the over molded backside of the reconfigured wafer will be realized by using PCB based redistribution technologies. A schematic illustration of the package is shown in Figure 2.

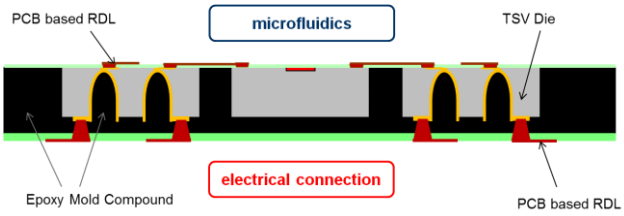

Figure 2. *Molded Reconfigured wafer with Silex TSV interposer and NXP biosensor is illustrated as a cross-section of the biosensor packaging with TSV interposer manufactured at Silex and molded together by FhG IZM.*

Future demands on even smaller size and lower cost will inevitably lead to requirements on totally integrated sensor solutions which are much smaller than today's available technology. The heterogeneous integration will serve many benefits, including less use of expensive Si material, yield improvements, and also the ability to integrate silicon dies fabricated in different technologies/fabs on different wafer dimensions. This will contribute to a low cost end product. Vertical chip stacking, often used in the heterogeneous integration, is realized by the metalized TSVs, is one alternative for decreasing the packaging size and the costs, since the volume and weight of the package is reduced. The TSVs enables shorter redistribution layers (RDL) and the smaller size means better performance since the signal travels a shorter route and parasitic capacitances decrease (which also impact system performance). Further, the overall size and power consumption of the device is decreased [4]. Additional benefits by using metalized TSVs in Si-substrate are that high RF performance and improved signal integrity can be obtained, as previously conducted work at Silex regarding metalized 50-90µm diameters rigid TSVs, have shown high RF performance with loss of a single coplanar TSV transition less than 0.04dB at 5GHz, which is considered to be very small [5]. These miniaturized rigid TSV Interposers with 50 µm diameter vias allows for I/O densities above 35 I/Os per mm^2.

The heterogeneous integration of the TSV interposer and the biosensor is achieved by reconfiguration wafer molding. There are two main approaches for embedded die technologies: *Wafer level integration*, where dies are embedded into polymer encapsulants and *3D vertical integration*, where dies are stacked on top of the substrate.

For wafer level integration there a many technology options being pursued worldwide. Main drivers are here the Embedded Wafer Level Ball Grid Array (eWLB) by Infineon [6] and the Redistributed Chip Package (RCP) by Freescale [7]. Whereas Amkor has focused on Through-Mold Via (TMV) package-on-package as industry standard and achieved via pitch of 400µm [8]. Fraunhofer IZM has demonstrated TMV technology for FOWLP vias down to 50µm diameter and 25µm pitch [9]. Singulated dies are assembled on an intermediate carrier and encapsulated by compression molding, forming a polymer wafer with embedded silicon dies. This "reconfigured" wafer is then released from the carrier. Using thin film technology, an electrical redistribution layer is routed on the wafer. Finally, the wafer is singulated by sawing into single packages containing multiple embedded Silicon dies. One trend in this fan-out wafer level packaging (FOWLP) technology is at the moment a double sided packaging with integration of vias through the encapsulants allowing electrical routing to the backside of the package [10].

Another concept for 3D integration of active components is the Chip in Polymer (CiP) technology, introduced by Fraunhofer IZM, TU Berlin and Wuerth [11]. It is based on embedding of ultra-thin dies into build-up layers of printed circuit boards (PCBs). The dies are bonded onto a core substrate using an adhesive; a resin coated copper (RCC) layer with thin Cu is used for the subsequent lamination. Interconnects are established by laser drilled micro vias (µ-via) followed by a PCB-compatible Cu plating [10]. The combination of both concepts, embedding into polymer by molding and redistribution by PCB technologies, has the potential for highly integrated low cost packages [12, 13].

TECHNICAL DESCRIPTION

Manufacturing of Bio-Sensors

The CMOS biosensor chip was designed by NXP Semiconductors in Belgium and the measurement principle is based on capacitive/impedance detection using metallic nanoelectrodes [14]. The biosensors were fabricated in a commercial available CMOS foundry process (at TSMC) on 300mm silicon substrates.

Prior to Chip in Polymer package processing, the CMOS biosensor wafer were thinned down to 300µm thickness and singulated into dies by NXP Semiconductors Germany.

Manufacturing of Metalized Through Silicon Vias Interposer

The metalized TSV is going to form the electrical connection between the microfluidics and the control unit located on different sides of the µ-fludic package. It is important that the metalized TSVs meets the requirements, such as low via resistance (<20mΩ), low losses and high yield (>90%) in order to meet performance and cost requirements of the end product. To minimize and reduce the risks of losses, the silicon substrate used was a 200mm diameter, 305µm thick

silicon wafers (3-10kΩ-cm) from Okmetic, Finland. The use of rigid interposers (300-430µm thick) will eliminate the ultrathin wafer handling requirements, such as bonding, debonding and carrier handling steps [15].

The TSVs were designed to have 200µm diameter via holes (BS) with 280 ±10 µm depth, giving the aspect ratio (AR) of 1.5:1. The decision was taken that there were no need to use smaller vias, with 50-90µm in diameter with pitch 150µm, giving ~16-32 vias/mm^2, which is available at Silex, since the landing pads for the µ-vias has to be as large as 100x100µm, due to potential die shift while assembling. Also, larger vias will ease the molding process and a higher yield is generally achieved, and lower cost of ownership is obtained.

The goal while DIRE etching the BS via is to achieve vias with straight or even re-entrant wall profile, to decrease the shadowing effect while deposition of a conformal seed layer. To be able to close the via and create hermetically sealed vias, a tapered structure should meet the BS via from the front side (FS), with dimensions of 25 ±10µm deep, surface opening 25 ±5µm and bottom 8 ±3µm, as shown in Figure 3.

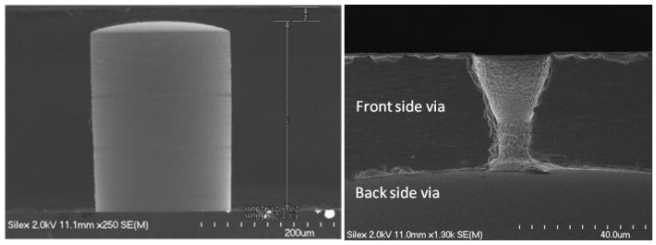

Figure 3. *SEM images of the finished DRIE optimization, LEFT: BS via hole; RIGHT: a close-up of the tapered shaped FS via meeting the BS via, to form an X-shaped locking TSV feature (XiVIA™).*

The X-shaped profile is also desired since it locks the structure and eases the complete void free Cu filling of the FS via. The FS via requires two DRIE steps, where anisotropic and isotropic etches has been used. All the used DRIE steps have been using Bosch-processes in a SPTS Pegasus or DSI chamber chambers, available at Silex Microsystems, with different optimized etching parameters in order to obtain the desired profiles.

To obtained high performance TSVs an insulation layer is deposited after the DRIE etching, consisting of 0.5µm thermal oxide and a 0.12µm LPCVD nitride. Before metallization could start a 0.5µm TiW adhesion/barrier layer was deposit with Oerlikon/Unaxis LLS sputter able to handle wafers with open through holes as well as a conductive 0.5µm Cu seed layer on both sides of the wafers. That deposition gives enough seedlayer coverage also deep inside the Via holes.

Early metalizing experiments were carried out on modified RENA and SemiTool Cu plating systems available at Silex 8" MEMS foundry line. However, the Cu plating results were not satisfying and non-conformal plating was obtained, with void present in the FS via, see Figure 4.

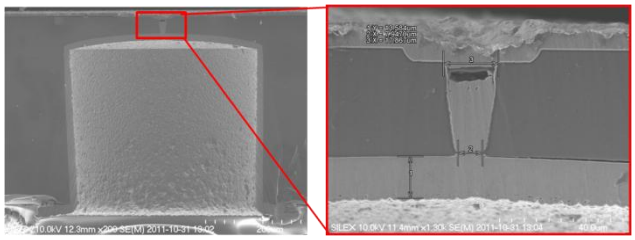

Figure 4. *Cross-sections of a Cu-plated TSV in the SemiTool Paragon single sided plating system, close-up image indicates voids in the FS via.*

A specially design plating tool, enabling cost effective simultaneous double sided plating of the TSVs, was therefore set-up. It was discovered that a double sided plating was preferred, since it minimized the risk of getting trapped air bubbles at the bottom of the BS via (where BS via meets FS via), due to the chemistry could flow through the via, until the FS hole is completely closed. The plating solution were a Cu-line fill chemistry provided by DOW and Enthone, and by proper mixing of the additives a conformal film along the BS via and void free hermetic sealing of the small FS via hole was obtained, see Figure 5. A line fill Cu-plating process is desired since Cu and Si have different CTE and also to limit the time-consuming Cu-plating. The used plating time to obtained controlled sealing and hermetic tight TSVs with the XiVIA™ feature is between 30-50 minutes. This plating time is a >20x reduction of the plating time used by Chen et. al. [16] for other similar TSV structures (300µm thick TSVs).

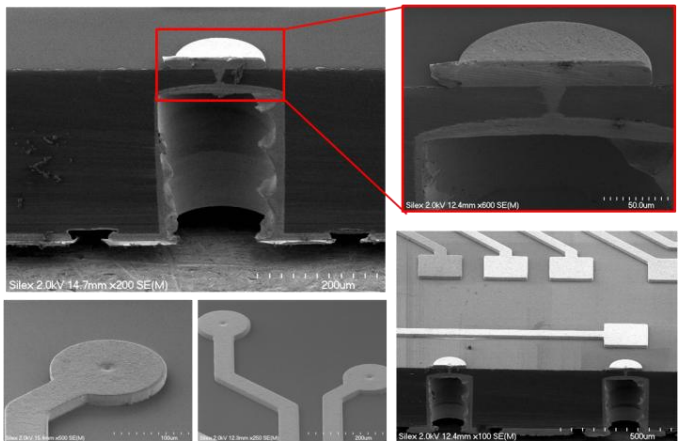

Figure 5. *Cross-section images taken with SEM at Silex. The upper right pictures shows a hermetically sealed TSV, it can be seen along the BS walls that the plated Cu is smeared during dicing process used to generate X-sections.*

Thick dry film resist (15µm) were used as plating mask for the Interposer redistributions layers (RDLs), creating line dimensions between with smallest Line/spacing of 40µm. For integration purposes in the later processing of µ-vias (see section "*Demonstrator Manufacturing*") the Cu layer must have a thickness in the range of 15-20µm to allow laser drilled µ-vias through the overmolded

backside of the interposer dies. Also, a thick Cu film will provide a low resistivity and good signal properties.
The yield of conformal plated vias was further increased by optimizing the pre-wetting steps, facilitating the wetting during plating. Also, the re-entrant wall profile of the BS and FS via will ease the wetting of the vias. Introduction of a quick Cu-etch step was necessary in order to remove potential formed copper oxide, which would decrease the adhesion of the electroplated Cu.

Evaluation of the plated vias was made by Scanning Electron Microscopy (SEM), however the Cu is soft and is easily smeared during cross sectional preparation using dicing, see Figures 5 and 6.

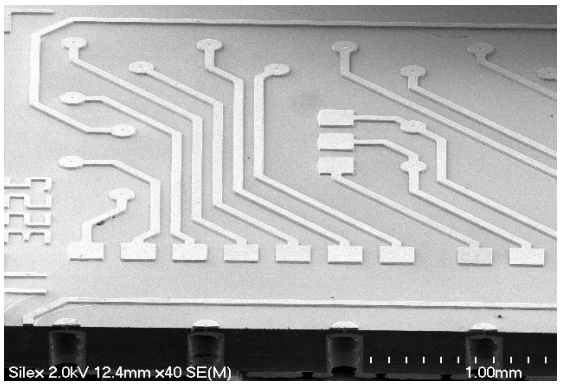

Figure 6. *A 3D bird's view of the finished TSV interposer die, with a cross section of the metalized TSV in the lower part of the image.*

Due to the Cu smearing while dicing, molded cross-section was prepared by FhG-IZM on small sample size and analysis shows a void free Cu-filling of the FS via as well as a conformal Cu-film along the BS walls. It was stated, in order to obtain a void free mold filling, vacuum molding was necessary, see Figure 7. This knowledge was then an important input for the full wafer molding using multiple dies for fabrication of re-configured wafers; see section "*Demonstrator Manufacturing*".

Figure 7. *Cross-section of the finished metalized TSVs. The left shows a non-vacuum molded cross-section where a void is obtained while the right picture shows a vacuum molded cross-section.*

The final step in manufacturing the metalized TSVs is to remove the conductive seed layer and the barrier layer to isolate the vias and create separated 3D connections between BS and FS. This is preferably done by wet single or double sided etching. The established process flow is presented in Figure 8.

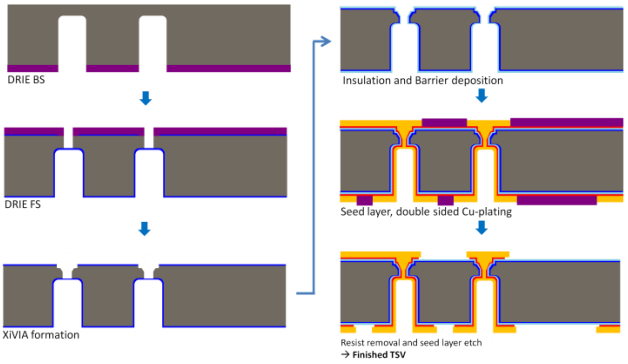

Figure 8*. Established Met-Via® process flow of the metalized TSV at Silex.*

TSV Interposer Layout

The interposer consists of 21 Met-Via®200 TSVs with a staggered 500µm pitch layout. On the back side (large via hole side) each via is routed to a 300x300µm^2 pad (µ-via landing pad for the later polymer wafer fabrication) along the die edge for easy fan-out and on the front side (small via hole side) each via is routed to a 200x200µm^2 pad (µ-via landing pad). The relatively large pads were chosen as the TSV dies will be fully covered with molding compounds from the backside and no optical alignment to the die and die pads is possible for RDL structuring. Therefore laser drilled through mold vias at the wafer edge were used as fiducials and front to backside alignment. Additionally, laser drilled blind vias through the EMC show a larger diameter an v-shape compared to through mold via due to the laser energy reflection in the via. Therefore more space meaning a larger pitch is needed between the blind vias. However, the TSV Interposer technology has the potential for higher via densities (>36 TSV/mm^2 using 150 µm TSV pitch [5]) and smaller pads (40x40 µm) if this is needed for the related application The routing on the back side is done with 100/75µm line/spacing while the front side uses 55/65µm line/space. The metallization for each via extends to a 75µm wide collar outside the via hole on the backside, see Figure 9.

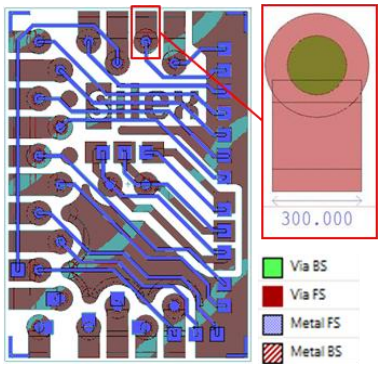

Figure 9. *CAD layout of the full Met-Via TSV interposer die and close-up of single TSV with µ-via landing pad.*

The resistance of the metalized TSVs was monitored by connecting the vias as a 'Daisy chain' where a series of 2-18 vias in an increment of 2 could be measured using low ohmic four-terminal measurements, see Figure 10.

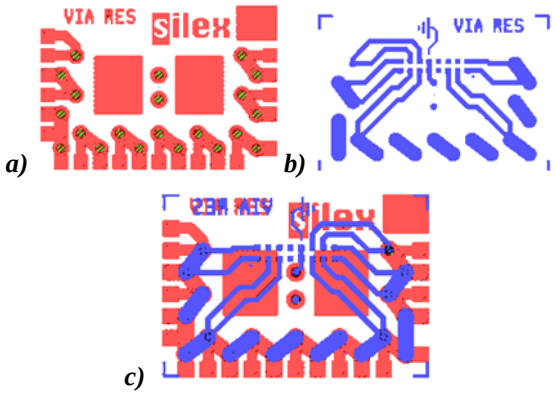

Figure 10. *CAD layout of the TSV Daisy chain (PCM test, a) back side layout, b) front side layout (4-terminals), c) view of all layers TSV Daisy chain.*

FAN-OUT WAFER LEVEL PACKAGING

The general process flow for the FOWLP approach with the metalized TSV interposers and CMOS biosensor chips die and PCB based redistribution starts with the lamination of an adhesive film to a carrier. This special adhesive film has one pressure adhesive side and one thermo-release side, i.e. by heating up the tape above a certain temperature, the thermo-release side of the tape loses its adhesion strength. On this carrier-adhesive film dies (the interposer TSV dies and the biosensor) are precisely placed, the active side facing down towards the intermediate carrier. High accuracy is needed as die pads have to match with the redistribution layer. Molding is done by large area compression molding. For chip redistribution, low cost PCB based technology with RCC has been selected. After lamination of the RCC film on both molded wafer sides in one step, µ-vias are drilled to the die pads on both sides of the wafer. Next process steps are cleaning, palladium activation and copper plating. By plating the die pad connection to the copper layers are achieved. Conductor line formation is done by laser direct imaging (LDI) in combination with a dry film resist and copper etching. The process steps described above are summarized in Figure 11.

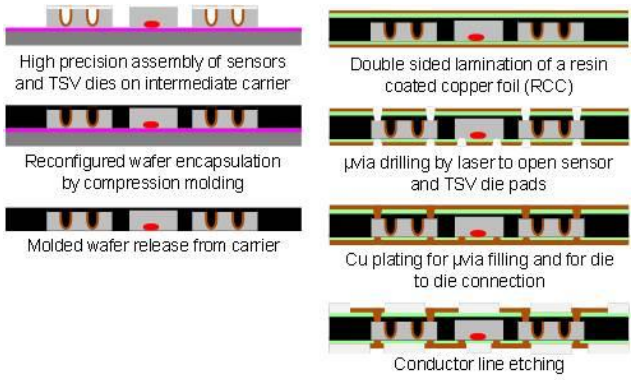

Figure 11. *FOWLP manufacturing flow at FhG-IZM used to interconnect CMOS bio-sensor with Met-Via TSV interposer dies for 3D electrical routing.*

Demonstrator Manufacturing

The general process flow described above was used for the fabrication of the CAJAL4EU biosensor package with electrical 3D routing obtained by Silicon TSV Interposers. Before die placement, a thermo-release film was laminated on a carrier. Release film was selected according to compression molding compound and the related molding temperature. A high speed chip assembly machine, Siplace CA3, was used for chip assembly with an accuracy of ± 15µm. Compression molding was done on a compression mold machine 120 t press from TOWA. For compression molding a liquid epoxy molding compound was selected with fine filler particles to allow the void free filling of the metal TSV interposer die structure. After wafer release from carrier die positions were measured with an optical measuring system Mahr OMS 600 to study the die shift and to adapt the drill and wiring layout according to the die placement accuracy and die shift during molding. Figure 12 shows a reconfigured molded wafer with biosensors and TSV interposer dies after carrier release.

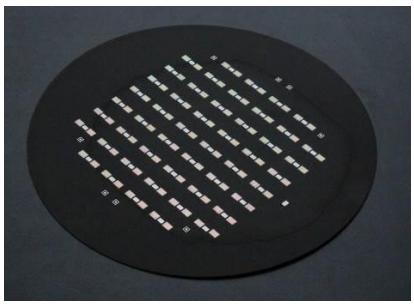

Figure 12. *Reconfigured molded 200 mm diameter wafer after carrier release.*

Cross-sections have been prepared to study the mold filling of the TSV interposer dies.
Figure 13 demonstrates that the fine filler molding compound in combination with the vacuum assisted compression molding allows the filling of the TSVs with 190µm diameter and a depth of 270µm without any air entrapments.

Figure 13. *Cross section of a part of the 5x3.5mm^2 TSV interposer die embedded in mold compound without any air entrapments present in any hollow TSV after compression molding step but before µ-via drilling and fan-out process steps.*

A filled RCC film with 5µm copper and 25µm resin was used as redistribution layer. Lamination was done in one step on both wafer sides under vacuum. µ-vias for chip connection were drilled in one step using a UV laser with an accuracy of ± 10µm. Next step was µ-via metallization

by Cu plating. Cu structuring is conducted by dry film resist lamination, laser direct imaging (LDI) which allows layout adaptation and die shift in mold compensation. Last process step was module singulation by dicing. Figure 14 shows a singulated module from top and bottom side.

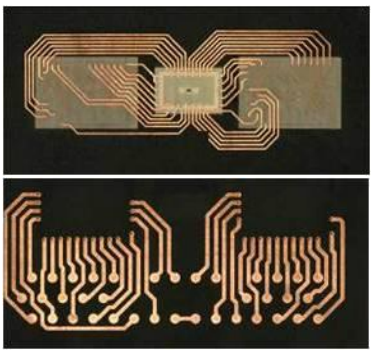

Figure 14. *Top-view photography of singular module after fan-out process steps with 40 I/Os form the CMOS die to two TSV dies with 21 TSV/die; a) top side to microfluidic, b) bottom side for electrical connection***.**

2D X-ray and X-ray CT analysis were performed to analyze and show interconnection integrity as well as 3D electrical routing from sensor top side to electrical connection on the bottom side. The x-ray CT image in Figure 15 nicely demonstrates the 3D routing in the module.

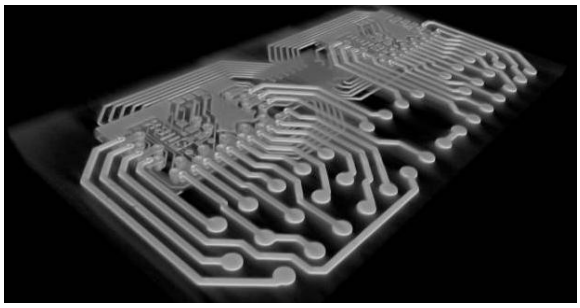

Figure 15. *X-ray CT image of a full module.*

The 2D X-ray image of the TSV die shown in Figure 16 demonstrates the three levels of 3D interconnections: µ-vias for connection of the top side of the TSV die, TSVs through the silicon and µ-vias for TSV backside connection through the molding compound.

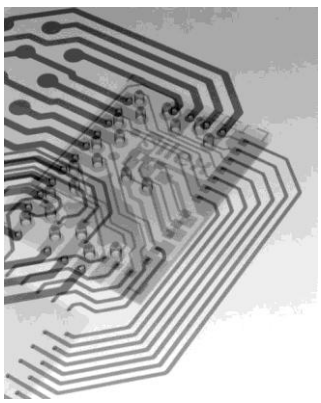

Figure 16. *X-ray image of a connected TSV die.*

Cross sections have been prepared to further analyze the 3D interconnection quality.

Figure 17 shows a detailed image of the cross section with the TSV die interconnection. The µ-via connection through the molding compound for backside interconnections as well as the µ-vias to the top side are well aligned to the die pads and show void-free metal connection to the die pads. The backside µ-via diameter is 100 µm giving an aspect ratio of <1:1.

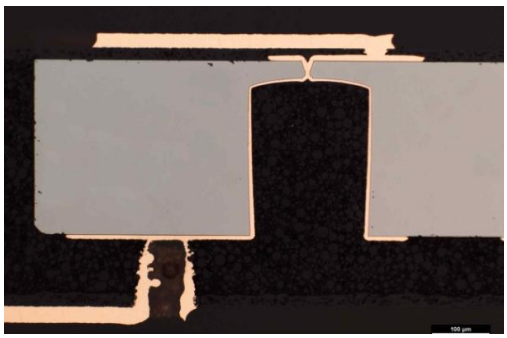

Figure 17. *Cross-section through the TSV die with all levels of 3D interconnects (RDLs both on Silicon and polymer levels).The µ-via through backside overmold with a thickness of approximately 80µm. Silicon thickness is 305 µm and TSV diameter is 200µm.*

CHARACTERIZATION

Electrical TSV Measurements

As mentioned before, a high yield is necessary in order to make a low cost product, therefore DC electrical measurements were conducted before sending the finished metalized TSV dies to Fraunhofer for molding. The via resistance was measured with a Agilent 34401A 6½ digit Multimeter and a Karl SUSS PM5 single side wafer probe station, using low ohmic four-terminal, where PCM die with via daisy chains according to Figure 10 were characterized. During the electrical characterization 42 different PCM dies from 7 different 200mm Si-wafers were measured (6 PCM die from each Si-wafer). On each PCM die 16 TSV were characterized which made a total of 672 TSVs. Only 3 out of the 672 TSVs showed short circuit or interruption, giving a yield of about 99.6 %. The same yield is expected for the sharp metalized TSV interposer dies (Figure 9). These Interposers are therefore usable for the being embedded in the reconfigurated polymer wafers allowing high packaging yield. Using a double sided wafer prober a selection of only good TSV Interposer dies could be perform which would increase the overall packaging yield even further. That's that main advantage with the heterogeneous assembly approach which allows for selection of only known good dies to be packaged and allowing wider selection of choices of CMOS processes for the biosensors than if TSV had been integrated directly into the CMOS dies. The metalized TSV were low ohmic with a resistance of 10.3 ±2.4mΩ/TSV (1-σ).

Electrical Measurements on Singulated Modules

The finalized singulated module (after the fan-out process step) with all levels of 3D interconnects (see Figures 14-17) were electrically characterized by measuring the resistance. The same equipment as for the electrical TSV measurements where used (Agilent 34401A 6½ digit Multimeter and a Karl SUSS PM5 probe station). Since the equipment lacks top to bottom side measurement, the fan-out routing had to be shorted at the top side with a conductive epoxy, see Figure 18, measuring the interconnections through the wafer twice (top-bottom-top). Preliminary electrical results indicates a resistance of ~1-3Ω, between the µ-vias on the bottom side through the TSV die (µ-vias landing pads and through the TSV) to the µ-via on the top side and back again.

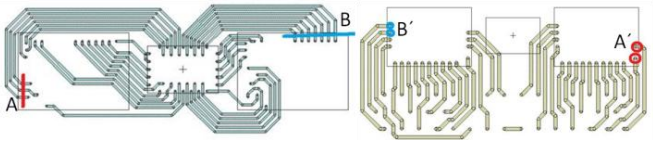

Figure 18. *CAD layout of the fan-out layer on the singulated module. Left image illustrating the top side fan-out layer where the A and B lines indicates where the fan-out redistribution layer was shorten. Right image showing the bottom side routing and A´ and B´ rings indicates the location of the probe needles.*

CONCLUSIONS

The metalized TSV interposer was successfully manufactured and PCM test structures were electrically characterized, showing a mean resistance of 10.3mΩ/Via (with σ of 2.4) and a yield of 99.6%. The TSV Interposer die was assembled together with the NXP bio-sensor die, where vacuum assisted compression molding of a liquid epoxy molding compound with fine filler particles realized void free filling of the TSV interposer die structure. Connections between the µ-vias landing pads on the TSV Interposer die and the fan-out redistribution layer were realized by laser drilling µ-vias and Cu-plating. The finished demonstrator module was optically inspected by X-ray CT, X-ray and SEM, all showing working connections. A preliminary electrical measurement also indicates that connections between the molded components with a resistance of ~1-3Ω is possible to obtain.

OUT LOOK FOR FUTURE RESEARCH AND COMMERCIALIZATION

The field of advanced package development, in recent years, has concentrated on heterogeneous IC packaging as a way of meeting the integration challenges of disparate technologies while simultaneously answering the needs for the market for smaller footprint, thinner packages which can deliver improvements in performance, size, and cost. Whether this has taken the form of 3D die stacking, 2.5D interposer technologies, functionally integrated LTCC substrates, package-on-package combinations or (as in this paper) WL reconstruction of Silicon dies embedded in polymer, all of these approaches aim to hit market points of size and performance at critical price points.

The development of commercially viable via alternatives has been a critical milestone in all of these packaging approaches. MEMS foundries like Silex, whose base technology involves deep etching and filling of materials for novel micro machined structures, has found its capabilities leveraged into the packaging space – something Yole Developpement coined in 2010 as the "emergence of the Mid-End foundry"[17].

The dual combination of wafer level reconstruction (FOWLP) and TMV/TSV, then, represent a novel and innovative way to circumvent the substantial engineering challenges of other, more direct, 3DIC approaches, and offers an approach which can be immediately employed to advanced IC packaging without substantial R&D or time to market penalties.

It is foreseen that the use of FOWLP technology will increase in order to meet the increased packaging needs for rapid growth in smart phone shipments [18]. For FOWLP future research will deal with up scaling of the processes presented to a larger scale moving from wafer scale to panel scale (Fan-out Panel Level Packaging FOPLP) for economic reasons, where the major challenges are placement accuracy on large area, low cost encapsulation over a large area and warpage control for such panels [19].

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